CLAIMS

1. A processing system for processing information efficiently and cost-effectively by switching between execution of time-critical and non-time-critical tasks comprising:

   a. a processing unit;

   b. a first register group coupled to said processing unit and including a first set of registers, said first register group for updating the status of said first set of registers, said processing unit reading the status of said first set of registers to execute time-critical tasks; and

   c. a second register group coupled to said processing unit and including a second set of registers, said second register group for updating the status of said second set of registers, said processing unit reading the status of said second set of registers to execute non-time-critical tasks, said processing unit switching to execute non-time-critical tasks by avoiding saving the status of said first set of registers,

   wherein said processing unit switches between executing time-critical tasks and non-time-critical tasks efficiently and cost-effectively by avoiding saving status of the first or second set of registers.

2. A processing system as recited in claim 1 wherein said processing unit switches to executing said time-critical tasks by avoiding saving the status of said second set of registers.

3. A processing system as recited in claim 1 further including a code random access memory (RAM) for storing instructions for execution of said time-critical tasks, said processing unit fetching instructions from said code RAM to execute said time-critical tasks.

4. A processing system as recited in claim 1 further including an instruction cache (I-cache) for storing instructions for execution of said non-time-critical tasks, said processing unit fetching instructions from said instruction cache to execute said non-time-critical tasks.

5. A processing system as recited in claim 1 further including a first data memory for storing data for executing said time-critical tasks, said processing system further including a second data memory for storing data for executing said non-time-critical tasks.

6. A processing system as recited in claim 1 further including a high priority interrupt controller responsive to interrupt commands requesting service, said high priority interrupt controller signaling said processing unit to provide service by executing said time-critical tasks.

7. A processing system as recited in claim 1 further including a low priority interrupt controller responsive to interrupt commands requesting service, said low priority interrupt controller signaling said processing unit to provide service by executing said non-time-critical tasks.

8. A processing system as recited in claim 5 further including a data bus bridge for transferring data from an external memory to said second data memory.

9. A processing system as recited in claim 1 wherein said processing system is in communication with a communication system, said processing system further including a register bus (R-bus) bridge for providing an interface between said processing system and said communication system.

10. A processing system as recited in claim 1 further including a real-time operating system (RTOS) for providing services for execution of said non-time-critical tasks.

11. A processing system as recited in claim 1 wherein said processing system is employed in an audio and video encoder/decoder (codec), said audio and video codec performing compression of audio data and video data to generate a compressed audio stream and a compressed video stream.

12. A processing system as recited in claim 11 wherein said non-time-critical tasks include multiplexing of said compressed audio stream with said compressed video stream, said time-critical tasks including providing video data for compression thereof.

13. A method for processing information efficiently and cost-effectively by switching between execution of time-critical tasks and non-time-critical tasks comprising:

updating the status of a first set of registers within a first register group;

reading the status of the first set of registers;

executing time-critical tasks;

updating the status of a second set of registers within a second register group;

reading the status of the second set of registers;

executing non-time-critical tasks; and

switching to execute non-time-critical tasks by avoiding saving the status of the first set of registers.

14. A processing system for processing information efficiently and cost-effectively by switching between execution of time-critical and non-time-critical tasks comprising:

a. a processing unit;

b. a first register group coupled to said processing unit and including a first set of registers, said first register group for updating the status of said first set of registers, said processing unit reading the status of said first set of registers to execute none-time-critical tasks; and

c. a second register group coupled to said processing unit and including a second set of registers, said second register group for updating the status of said second set of registers, said processing unit reading the status of said second set of registers to execute time-critical tasks, said processing unit switching to execute time-critical tasks by avoiding saving the status of said first set of registers,

wherein said processing unit switches between executing time-critical tasks and non-time-critical tasks efficiently and cost-effectively by avoiding saving status of the first or second set of registers.

15. A processing system as recited in claim 14 wherein said processing unit switches to executing said non-time-critical tasks by avoiding saving the status of said second set of registers.

16. A processing system as recited in claim 14 further including a code random access memory (RAM) for storing instructions for execution of said time-critical tasks, said processing unit fetching instructions from said code RAM to execute said time-critical tasks.

17. A processing system as recited in claim 14 further including an instruction cache (I-cache) for storing instructions for execution of said non-time-critical tasks, said processing unit fetching instructions from said instruction cache to execute said non-time-critical tasks.

18. A processing system as recited in claim 14 further including a first data memory for storing data for executing said time-critical tasks, said processing system further including a second data memory for storing data for executing said non-time-critical tasks.

19. A processing system as recited in claim 14 further including a high priority interrupt controller responsive to interrupt commands requesting service, said high priority interrupt controller signaling said processing unit to provide service by executing said time-critical tasks.

20. A processing system as recited in claim 14 further including a low priority interrupt controller responsive to interrupt commands requesting service, said low priority interrupt controller signaling said processing unit to provide service by executing said non-time-critical tasks.

21. A processing system as recited in claim 18 further including a data bus bridge for transferring data from an external memory to said second data memory.

22. A processing system as recited in claim 14 wherein said processing system is in communication with a communication system, said processing system further including a register bus (R-bus) bridge for providing an interface between said processing system and said communication system.

23. A processing system as recited in claim 14 further including a real-time operating system (RTOS) for providing services for execution of said non-time-critical tasks.

24. A processing system as recited in claim 14 wherein said processing system is employed in an audio and video encoder/decoder (codec), said audio and video codec performing compression of audio data and video data to generate a compressed audio stream and a compressed video stream.

25. A processing system as recited in claim 24 wherein said non-time-critical tasks include multiplexing of said compressed audio stream with said compressed video stream, said time-critical tasks including providing video data for compression thereof.

26. A method for processing information efficiently and cost-effectively by switching between execution of time-critical tasks and non-time-critical tasks comprising:

updating the status of a first set of registers within a first register group;

reading the status of the first set of registers;

executing non-time-critical tasks;

updating the status of a second set of registers within a second register group;

reading the status of the second set of registers;

executing time-critical tasks; and

switching to execute time-critical tasks by avoiding saving the status of the first set of registers.